Patent claims

1. Parallel databus having a plurality of parallel signal lines to which a plurality of assemblies (2) can be connected, whereby each assembly (2) has a databus driver being in immediate connection with the signal lines and has a controller (4) that is connected to the databus driver (3), whereby a sub-number of the signal lines represent data lines for transmitting the data and control lines for controlling the data transmission of the data via the data lines, and a clock generator for generating a predetermined bus frequency, with which the signals transmitted in the signal lines are clocked, characterized in that the databus drivers (3) are connected to the clock generator and the databus drivers (3) are fashioned such that the signals to be transmitted from and to the data and control lines are accepted during a clock pulse prescribed by the clock generator, and are emitted during a following clock pulse.

2. Parallel databus according to claim 1, characterized in that the clock generator generates a bus frequency of at least 20 MHz.

3. Parallel databus according to claim 2, characterized in that the clock generator generates a bus frequency of approximately 40 MHz

4. Parallel databus according to one of the claims 1 to 3, characterized in that the databus has 32 data lines.

5. Parallel databus according to one of the claims 1 to 4,

characterized in that

a further sub-number of the signal lines are fashioned as decision lines for deciding which assembly connected to the signal lines has access priority, whereby the decision lines are connected to non-clocked open-drain outputs of the respective databus drivers (3), so that they form a wired-or logic.

6. Parallel databus according to claim 5,

characterized in that

a device for generating an auxiliary clock pulse (BCLK2 with a lower frequency than the bus frequency is provided for driving the decision lines.

7. Parallel databus according to claim 6,

characterized in that

the device for generating an auxiliary clock pulse is a frequency divider.

8. Parallel databus according to one of the claims 1 to 7,

characterized in that

the outputs of the databus driver (3) leading to the controller (4) are fashioned as low-voltage TTL outputs.

9. Parallel databus according to one of the claims 1 to 8,

characterized in that

the signal lines have a physical expanse of at least 40 cm.

10. Parallel databus according to one of the claims 1 to 8,

characterized in that

the signal lines have a physical expanse of at least 50 cm.

11. Parallel databus according to one of the claims 1 to 10,

characterized in that

a plurality of the assemblies (2) that are connected to the signal lines are respectively provided with a processor.

12. Parallel databus according to one of the claims 1 to 11,
characterized in that
the databus (5) is multibus-compatible.

13. Method for the communication of two assemblies (2), which are each connected to a processor, by means of a parallel databus (5) according to one of the claims 1 to 12, whereby data packets (messages) are exchanged between the two assemblies (2),
characterized in that
each data packet is acknowledged by only one single handshake.

14. Method according to claim 13,
characterized in that
a handshake respectively comprises a data-ready signal (SCN3) of the transmitter assembly (2) and a data-ready signal (SCN4) of the receiver assembly (2), whereby the data-ready signal (SCN3) of the transmitter assembly (2) is sent to the receiver assembly (2) at the beginning of the data transfer, and the receiver assembly sends its data-ready signal (SCN4) to the receiver assembly (2) after the data-ready signal (SCN3) of the transmitter assembly (2) has been received.

15. Method according to claim 14,
characterized in that
the transmitter assembly (2) only sends its data-ready signal (SCN3) when the complete data packet is present on this assembly (2).

16. Method according to claim 14 or 15,
characterized in that
the maximum size of the data packets is set to a predetermined value, and

the receiver assembly (2) only sends its data-ready signal (SCN4) when there is sufficient storage space on the receiver assembly (2).

17. Method according to claim 16,
c h a r a c t e r i z e d i n t h a t
32 byte, 64 byte, 96 byte or 128 byte are determined as the maximum size of the data packets.

18. Printer control unit for high-performance printers having
an I/O-module, one or more raster modules (9) and a serializer module (10), whereby the modules (8 to 10) each have a processor,
c h a r a c t e r i z e d i n t h a t
the modules are connected to a parallel databus according to one of the claims 1 to 12.

Add B1 Abstract